

Notice of References Cited	Application/Control No. 10/724,277		Applicant(s)/Patent Under Reexamination MCGAUGHY ET AL.	
	Examiner Shambhavi Patel		Art Unit 2128	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,807,520	10-2004	Zhou et al.	703/14
*	B	US-6,026,226	02-2000	Heile et al.	716/12
*	C	US-6,339,836	01-2002	Eisenhofer et al.	716/5
*	D	US-6,807,520	10-2004	Zhou et al.	703/14
*	E	US-6,577,992	06-2003	Tcherniaev et al.	703/14
*	F	US-2004/0078767	04-2004	Burks et al.	716/008
*	G	US-2003/0237067	12-2003	Mielke et al.	716/6
*	H	US-6,449,761	09-2002	Greidinger et al.	716/11
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Jones et al. 'A Cache-Based Method for Accelerating Switch-Level Simulation'. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems: Vol. 13, No. 2 February 1994.			
	V	Wong, Yiwan. 'Hierarchical Circuit Verification'. IEEE 22 nd Design Automation Conference. 1985.			
	W				
	X				

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.